

Serial No.: 09/829,161

**REMARKS**

No new matter has been added. The Applicant again requests entry of the amendments as set forth in the Appendices hereto prior to examination of the application on the merits.

Respectfully submitted,



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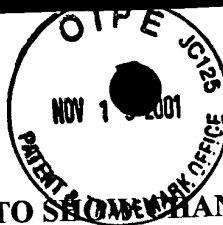
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## **APPENDIX D**

**(VERSION OF CLAIMS AS AMENDED HEREIN  
WITH MARKINGS TO SHOW CHANGES MADE)**

**(Serial No. 09/829,161)**



VERSION OF CLAIMS WITH MARKINGS TO SHOW CHANGES MADE

1. (Amended) A method for making a metallization structure for a semiconductor device, comprising:

forming a substantially planar first dielectric layer on a substrate;  
forming at least one metal layer over the first dielectric layer;  
forming a conducting layer over the at least one metal layer;  
forming a second dielectric layer over the conducting layer;  
removing aligned portions of the second dielectric layer, conducting layer, and at least one metal layer to form a [multi-layer]multilayer structure; and  
forming metal spacers on sidewalls of the [multi-layer]multilayer structure.

4. (Amended) The method of claim 3, further including forming a second metal layer between [the]a first metal layer of said at least one metal layer and the substrate[ and], said second metal layer comprising TiN, TiW, WN, or TaN.

11. (Amended) The method of claim 1, [further comprising]wherein said forming a second dielectric layer comprises forming [a]the second dielectric layer on the conducting layer to have sidewalls aligned with sidewalls of the [conductive]conducting layer[ sidewalls], and forming the metal spacers to extend along the sidewalls of the second dielectric layer.

12. (Amended) The method of claim 11, further comprising forming the second dielectric layer of a low dielectric constant material.

13. (Amended) The method of claim 12, further comprising forming the second dielectric layer of a fluorine-doped silicon oxide.

16. (Amended) The method of claim 1, further comprising forming the at least one metal layer by CVD, PVD or PECVD.

21. (Amended) The method of claim 1, wherein removing aligned portions of the second dielectric layer, conducting layer, and at least one metal layer to form [a multi-layer]the multilayer structure is effected by patterning and etching the second dielectric layer, the conducting layer, and the at least one metal layer.

22. (Amended) The method of claim 1, further comprising forming the metal spacers by forming a metal spacer layer over the [multi-layer]multilayer structure and first dielectric layer and removing portions thereof overlying the first and second dielectric layers.

23. (Amended) The method of claim 22, further comprising forming the metal spacer layer over the [multi-layer]multilayer structure and first dielectric layer by a conformal deposition process.

24. (Amended) The method of claim 23, wherein [the ]portions of the metal spacer layer over the [multi-layer]multilayer structure and first dielectric layer are removed by etching.

26. (Amended) The method of claim 25, further comprising removing any remaining portion of the second dielectric layer and upper portions of the metal [spaces]spacers by etching.

27. (Amended) A method for making a metallization structure comprising:  
forming a substrate comprising at least one metal layer on [the]a surface thereof;  
forming a dielectric layer over the at least one [the ]metal layer;  
forming an aperture having at least one sidewall through the dielectric layer to expose a surface of  
the at least one metal layer;  
forming a metal spacer on the at least one sidewall of the aperture; and  
forming a conductive layer in a remaining portion of the aperture.

30. (Amended) The method of claim 29, wherein the at least one metal layer comprises a first metal layer, and further [including]comprising forming a second metal layer between the first metal layer and the substrate[ and], said second metal layer comprising TiN, TiW, WN, or TaN.

34. (Amended) The method of claim 27, further comprising forming the [conducting]conductive layer by vapor deposition.

35. (Amended) The method of claim 34, further comprising forming the [conducting]conductive layer by CVD, PVD or PECVD.

49. (Amended) A method for making a metallization structure comprising:  
forming a substrate comprising at least one metal layer on [the]a surface thereof;  
forming a dielectric layer over the at least one metal layer;  
forming an aperture through the dielectric layer to expose a surface of the at least one metal layer;  
forming a conducting layer in the aperture;  
forming at least one upper metal layer overlying the dielectric layer and the conducting layer in the aperture;  
removing portions of the at least one upper metal layer overlying the dielectric layer, removing the dielectric layer, and removing portions of the at least one metal layer surrounding the conducting layer to form a [multi-layer]multilayer metal structure having at least one sidewall; and  
forming a metal spacer on the at least one sidewall of the [multi-layer]multilayer metal structure.

52. (Amended) The method of claim 51, wherein the at least one metal layer comprises a first metal layer, and further including forming a second metal layer between the first metal layer and the substrate[ and], said second metal layer comprising TiN, TiW, WN, or TaN.

59. (Amended) The method of claim 49, further comprising forming the metal spacer by vapor deposition of a metal layer over the [multi-layer]multilayer metal structure and directional etching of the vapor-deposited metal layer.

62. (Amended) The method of claim 49, further comprising forming the at least one upper metal layer [on the conducting layer]overlying the dielectric layer from Ti, Ta, W, Co or Mo or an alloy or a compound of any thereof, including TaN or TiN.

70. (Amended) The method of claim 49, further comprising forming the at least one metal layer, metal spacer, and at least one upper metal layer of the same metal.

71. (Amended) The method of claim 70, wherein the same metal is Ti.

## ABSTRACT OF THE DISCLOSURE

The present invention provides a metallization structure for semiconductor device interconnects such as a conductive line, including a substrate with a substantially planar upper surface, foundation metal layer disposed on a portion of the substrate upper surface, primary conducting metal layer overlying the foundation metal layer, and metal spacer on the sidewalls of the primary conducting metal layer and the foundation metal layer. The present invention also provides a metallization structure including a substrate with a foundation metal layer disposed thereon, a dielectric layer with an aperture therethrough being disposed on the substrate, where the bottom of the aperture exposes the foundation metal layer of the substrate, and a metal spacer on the sidewall of the aperture and a line or plug of a primary conducting metal fill the remaining portion of the aperture. The present invention also includes methods for making the metallization structures.

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